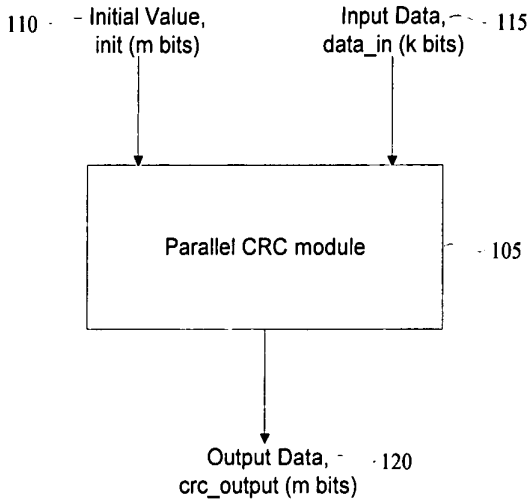
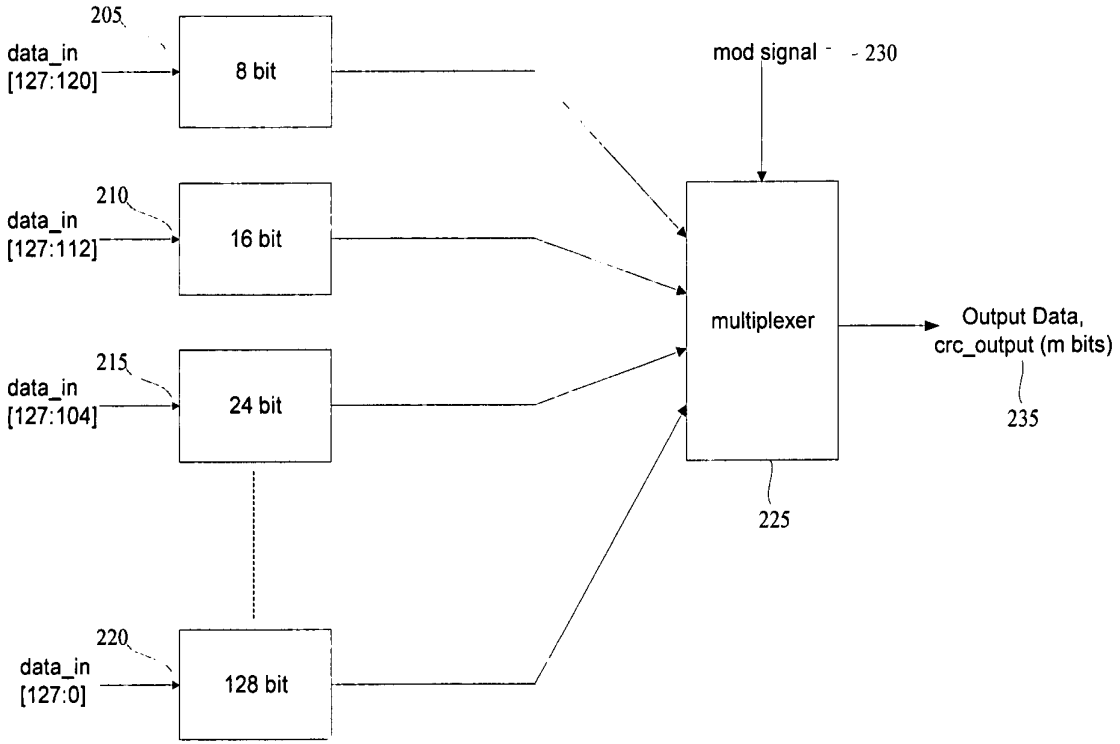

110
Initial Value,
init (m bits)
Input Data,
data_in (k bits)
115
Parallel CRC module
105
Output Data,
crc_output (m bits)
120

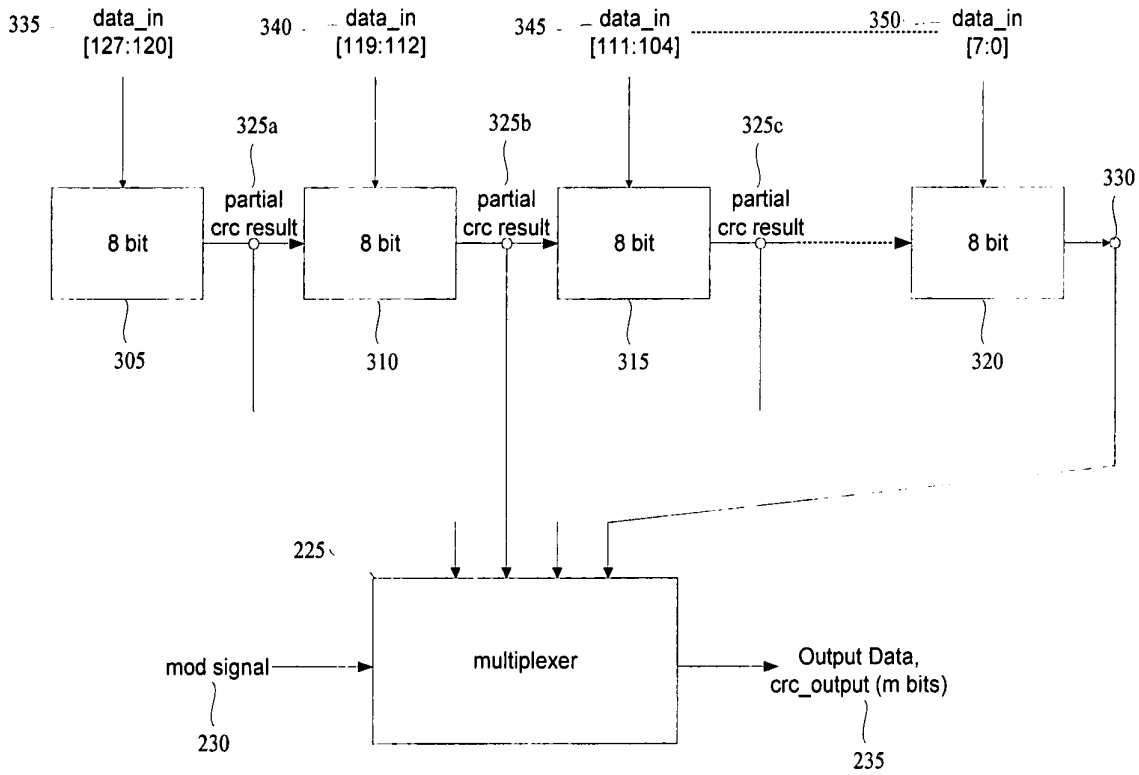
100

Figure 1


205
data_in
[127:120]
8 bit
mod signal
230
210
data_in
[127:112]
16 bit
multiplexer
Output Data,
crc_output (m bits)
215
data_in
[127:104]
24 bit
235
225
220
data_in
[127:0]
128 bit

200

Figure 2


335
data_in
[127:120]
340
data_in
[119:112]
345
data_in
[111:104]
350
data_in
[7:0]
325a
325b
325c
330
partial
crc result
partial
crc result
partial
crc result
8 bit
8 bit
8 bit
8 bit
305
310
315
320
225
multiplexer
mod signal
230
Output Data,
crc_output (m bits)
235

300

Figure 3

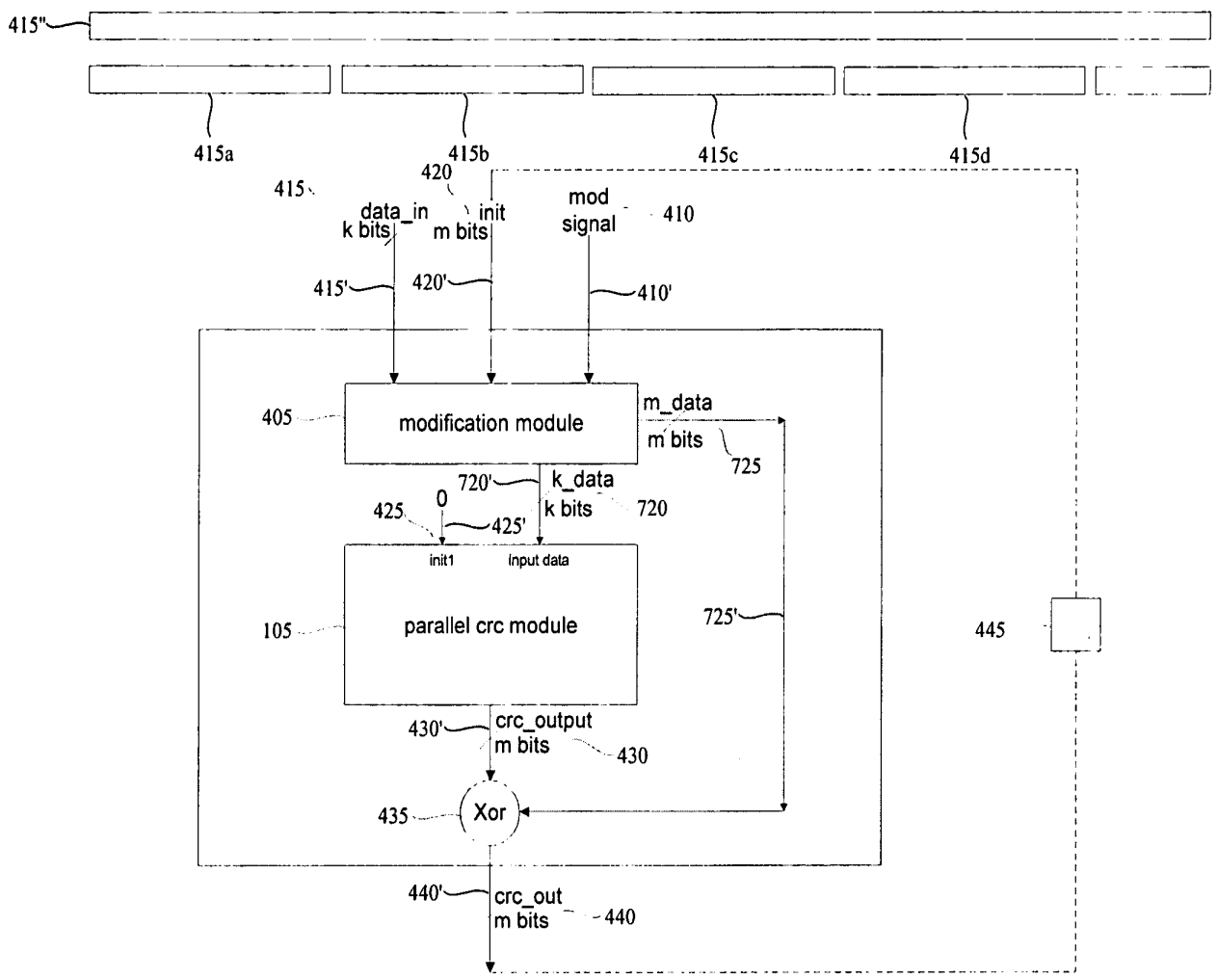

415"
415a
415b
415c
415d
415
420
data_in
k bits
init
m bits
mod
signal
410
415'
420'
410'
405
modification module
m_data
m bits
725
720'
k_data
k bits
720
425
0
425'
init1
Input data
105
parallel crc module
725'
445
430'
crc_output
m bits
430
435
Xor
440'
crc_out
m bits
440
400

Figure 4

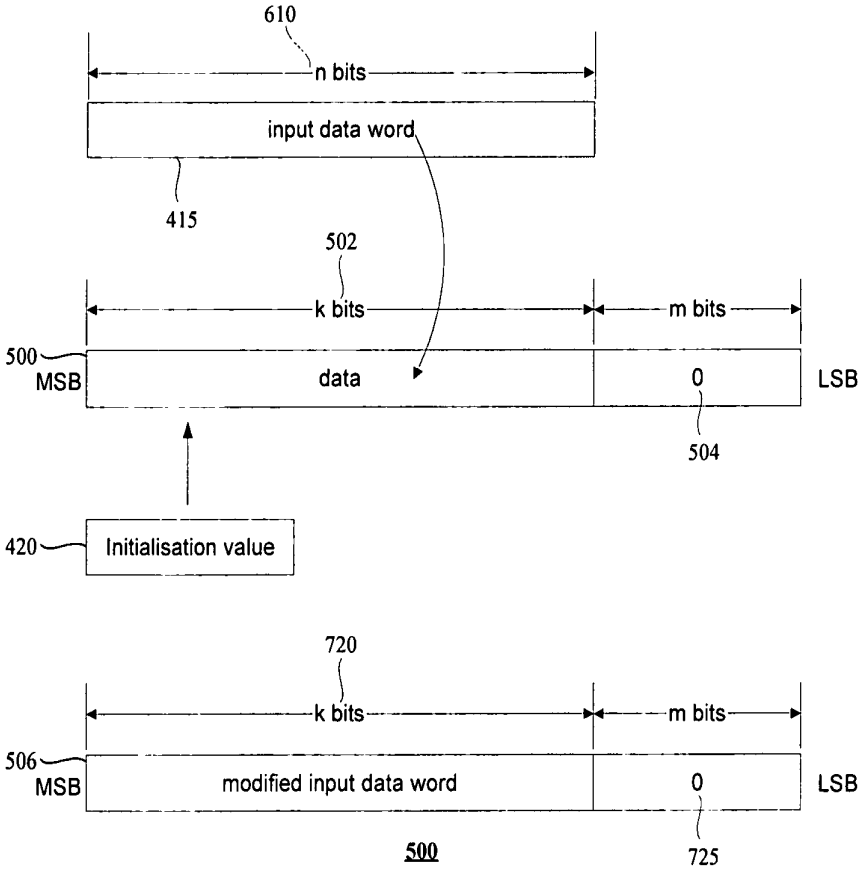

610
n bits
input data word
415
502
k bits
m bits
500
MSB
data
0
LSB
504
420
Initialisation value
720
k bits
m bits
506
MSB
modified input data word
0
LSB
500
725

Figure 5

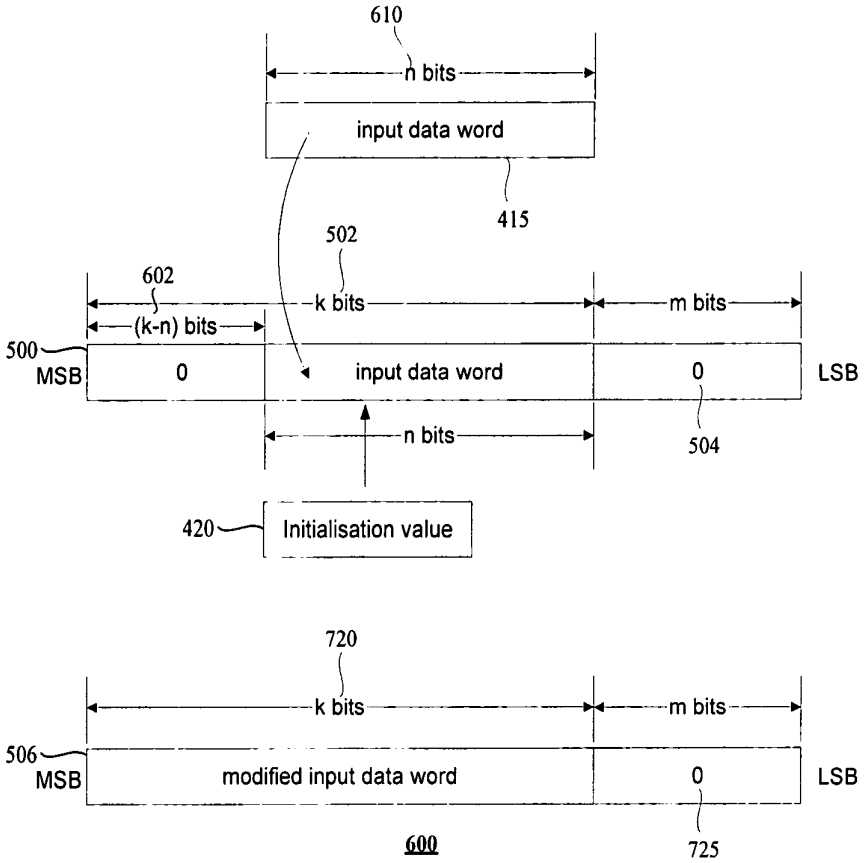

610
n bits
input data word
415
502
602
k bits
m bits
(k-n) bits
500
MSB
0
input data word
0
LSB
n bits
504
420
Initialisation value
720
k bits
m bits
506
MSB
modified input data word
0
LSB
600
725

Figure 6

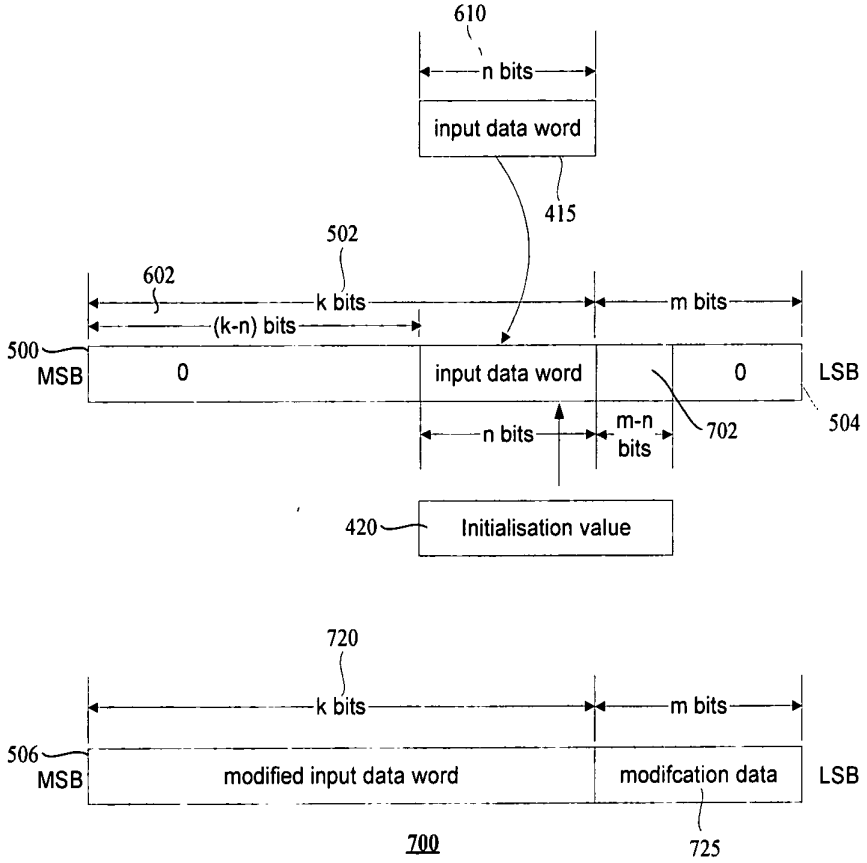

610
n bits
input data word
415
502
602
k bits
m bits
(k-n) bits
500
MSB
0
input data word
0
LSB
504
n bits
m-n bits
702
420
Initialisation value
720
k bits
m bits
506
MSB
modified input data word
modifcation data
LSB
700
725

Figure 7

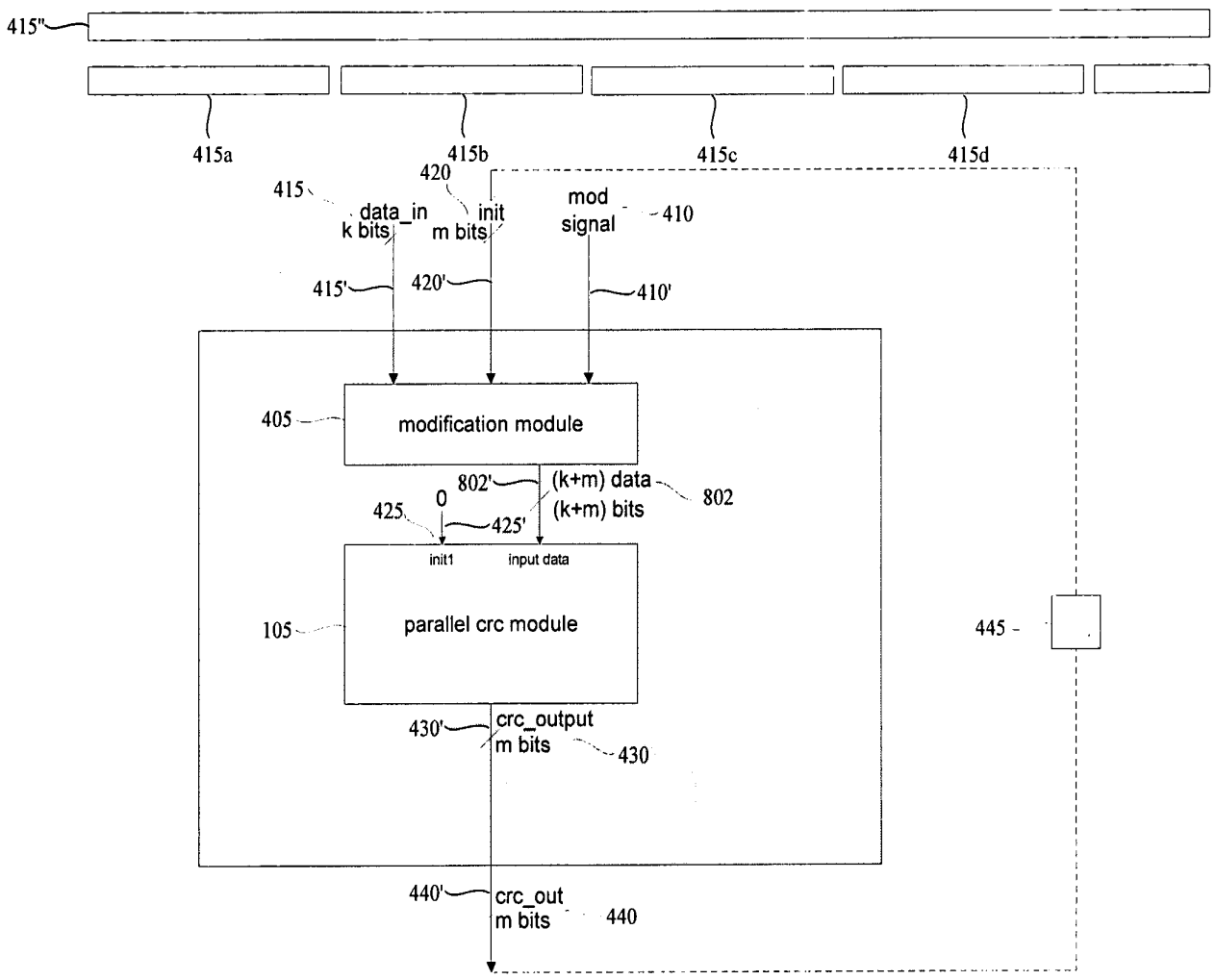

415"
415a
415b
415c
415d
420
415
data_in
k bits
init
m bits
mod
signal
410
415'
420'
410'
405
modification module
802'
(k+m) data
802
0
(k+m) bits
425
425'
init1
input data
105
parallel crc module
445
430'
crc_output
m bits
430
440'
crc_out
m bits
440
800

Figure 8